A "Winner-Take-All" IC for Determining the Crystal of Interaction in PET Detectors*

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Abstract

We present performance measurements of a "Winner-Take-All" (WTA) CMOS integrated circuit to be used with a pixel based PET detector module. Given *n* input voltages, it rapidly determines the input with the largest voltage, and outputs the encoded address of this input and a voltage proportional to this largest voltage. This is more desirable than a threshold approach for applications that require exactly one channel to be identified or when noise is a significant fraction of the input signal. A sixteen input prototype has been fabricated using two 1.2 µm processes (HP linear MOS capacitance and Orbit double–poly capacitance). ICs from both processes reliably identify (within 50 ns) the maximum channel if ΔV (the difference between the two highest channels) is >20 mV.

The key element in the WTA circuit is an array of high gain non-linear current amplifiers. There is one amplifier for each input channel, and each amplifier is composed of only two FETs. All amplifiers are supplied by a common, limited current source, so the channel with the largest input current takes all of this supply current while the other channels receive virtually none. Thus, these amplifier outputs become a set of logical bits that identify the maximum channel, which is encoded and used to select a multiplexer input. A voltage to current converter at each input channel turns this into a voltage sensitive device. This circuit uses very little power, drawing approximately 100 µA at 5 V.

I. INTRODUCTION

We are designing a PET (positron emission tomography) detector module to identify 511 keV photons from positron annihilation with good spatial and temporal resolution [1, 2]. This design consists of an 8 by 8 array of 3 mm square by 30 mm deep BGO scintillator crystals coupled on one end to a single photomultiplier tube and on the opposite end to a 8 by 8 array of 3 mm square silicon photodiodes. The photomultiplier tube provides an accurate timing pulse and initial energy discrimination for the 64 crystals in the module, while the silicon photodiode array identifies the crystal of interaction.

Because of the high data rates (up to 10^6 Hz per detector module), it is imperative that a *single* photodiode pixel be rapidly assigned (≤100 ns) as the crystal of interaction whenever the photomultiplier tube triggers. The signal to noise ratio in the photodiode is small — typically a 700 e^- signal for a full 511 keV energy deposit and a 125 e^- RMS noise. Compton interactions cause events with energy deposited in more than one pixel, increasing the complexity of the event topology and further reducing the signal to noise ratio. Under these conditions, a simple threshold scheme will frequently have zero or greater than one pixels above threshold, yielding ambiguous events. Therefore, we have designed a "Winner-Take-All" (WTA) circuit to rapidly identify the maximum pixel. This circuit performs a function similar to WTA circuits used in neural network applications [3, 4], but uses a new design that requires significantly fewer components.

II. CIRCUIT DESIGN

A conceptual diagram of the WTA circuit is shown in Figure 1. Each input voltage is converted to a current proportional to this voltage and sent to the WTA circuit, whose main component is an array of *n* identical FETs whose gates and sources are tied together. The current proportional to the input voltage of channel *i* is applied to the drain of FET *i*, and since these FETs have common gates and sources, the FET with the highest drain current establishes a common operating point for all these transistors and determines V_{GS}.

These transistors have high output conductance, as shown schematically in the IV curve in Figure 2. Thus, Ii_{In} defines V_{Di}. and relatively small differences between the drain currents are transformed into relatively large differences between the drain voltages. The drain of each of these input FETs is connected to the gate of an output FET which, given an unlimited current supply, would produce an output current proportional to the square of the input voltage (minus an offset) and further magnify the differences between input levels. However, all of these output FETs are supplied by a common, limited (30 µA) supply. Therefore, the channel with the highest input voltage (the winner) will take the entire output supply current, yielding one output with the entire supply current and the remainder with no output current. These output currents are used as logical bits identifying the maximum channel. Note that once the voltage to current conversion has been performed, only two transistors are required for each input channel. The

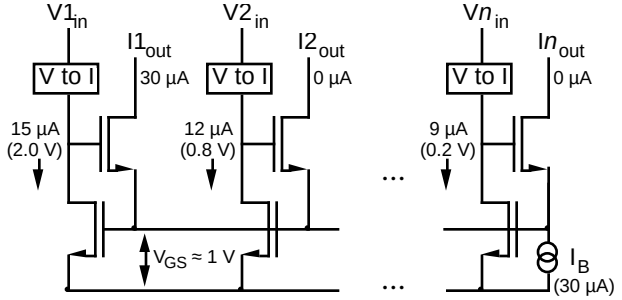

Figure 1: Conceptual design of the circuit that identifies the input with the maximum voltage. Values for current or voltage are from simulation and are only used to illustrate the design concept.

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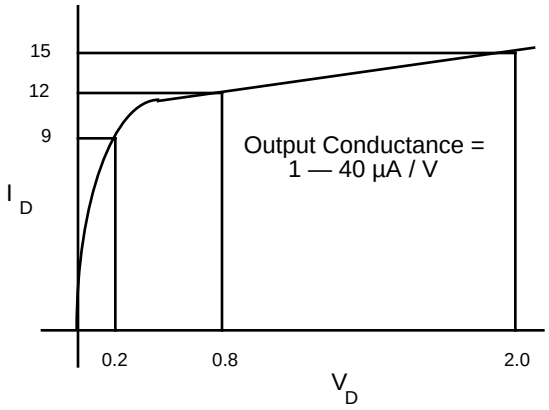

Figure 2: Conceptual diagram of the IV curve for the high output conductance input FETs in this design. Values for I or V are taken from simulation and are only used to illustrate the design concept.

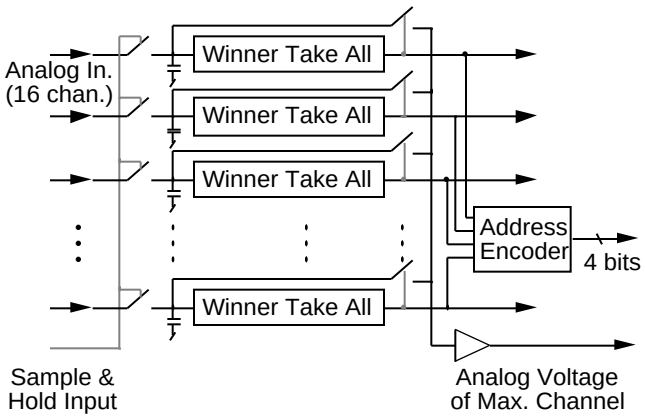

Figure 3: Block diagram of the WTA integrated circuit.

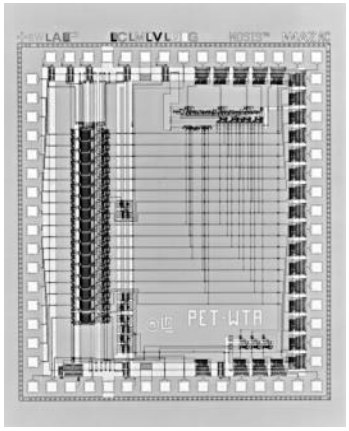

Figure 4: Photograph of the 16 channel prototype integrated circuit. The WTA portion is the vertical stripe (approximately 0.3 x 1.6 mm) along the left edge, while the encoder is in the upper right hand corner. The size of the chip is roughly 2 mm x 3 mm.

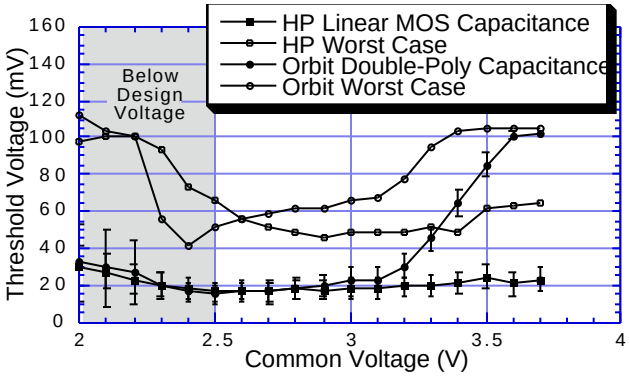

Figure 5: Average and worst case threshold voltages (averaged over all channels of all chips) as a function of common voltage.

total current drawn is roughly 100 µA at 5 V and is independent of the number of input channels, as 30 µA goes to the shared current supply of the WTA and the remaining 70 µA is drive current for the output bits. The limiting factor in this design is the uniformity of the input FET offset voltages.

The IC fabricated (Figure 3) has additional components to facilitate use. Each voltage input has a sample and hold circuit actuated by a common logic input to allow all inputs to be strobed simultaneously. Although the individual logical output bits are provided, an address encoder is also included to provide redundant data in a more compact format. Finally, an analog multiplexer combined with an output buffer provides an output voltage that is proportional to the maximum input voltage.

III. Circuit Performance

Sixteen input channel prototypes were fabricated using two 1.2 µm processes (HP linear MOS capacitance and Orbit double–poly capacitance). A photograph of the resulting IC (Figure 4) shows that the physical size of the WTA circuit is small — approximately 0.03 mm^2. In order to maintain compatibility with the DC output voltage of the shaper amplifier that proceeds it [5], a 2.5 V input voltage corresponds to baseline input signal, thus the dynamic range of input voltages is from 2.5 to 4.0 V. Of the 15 prototype chips produced with the HP process, all portions of the circuit performed reliably for 14 chips. Of the chips produced with the Orbit process, the WTA portion of the circuit performed reliably on 7 of the 9 chips, but the address encoder and analog output buffer failed to perform on any of these chips. It is not known whether this failure was due to a design error or a processing error.

These devices were characterized by supplying 15 of the inputs with a *common voltage* and the 16^{th} input with a test voltage. The voltage difference ΔV between these two voltages is gradually reduced until the first incorrect address is detected, indicating that the wrong input is identified as the maximum. For the HP devices, either the 16 digital outputs or the 4 encoded output bits could be used to determine the address (both gave identical results) — only the 16 digital outputs could be used for the Orbit devices. This minimum ΔV necessary for accurate performance is defined to be the *threshold voltage* for a single measurement. Figure 5 plots the mean threshold voltage (averaged over all channels on all chips) as a function of common voltage for the two processes, as well as the "worst case" threshold voltage (*i.e.* the largest threshold voltage found on any channel).

For common voltages above 2.5 V, the mean voltage difference required for accurate identification is ΔV=19 mV

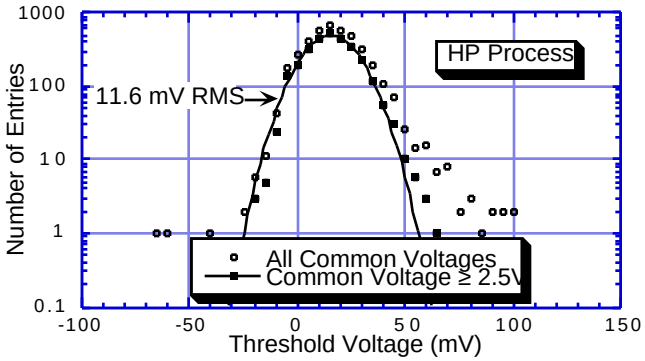

Figure 6: Distribution of threshold voltages collected over all channels of all chips (HP process only) at all common voltages.

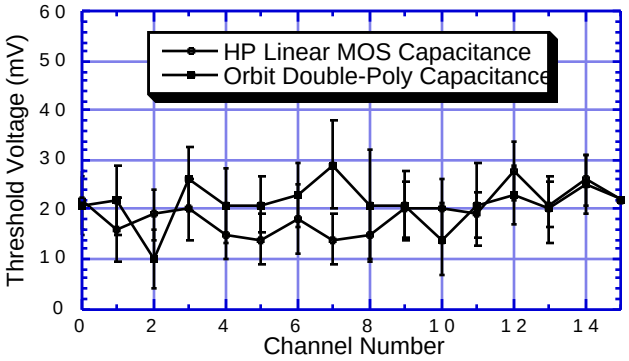

Figure 7: Mean threshold voltage (averaged over all chips at all common voltages) versus channel number.

(with an RMS deviation of 11.6 mV) for the HP process and the "worst case" threshold voltage is typically below 60 mV. As the WTA circuit is essentially a current input circuit, this threshold of 19 mV corresponds to a 3 µA input current difference. For common voltages below the 2.5 V design voltage, the performance is slightly degraded but the circuit still operates reasonably well. The prototypes fabricated with the 1.2 µm Orbit double–poly capacitance process show similar properties, although Figure 5 shows that the threshold voltage increases significantly when the common voltage is above 3.1 V. This increase in threshold voltage is likely to be caused by nonlinearity (and hence limited dynamic range) in the MOS resistor used to perform the input voltage to current conversion. The larger nonlinearity in the Orbit chips may be due to unfavorable process parameters in this particular Orbit run (note that difficulties were also observed in the encoder and output buffer of the chips), as the designs submitted to HP and Orbit had identical dimensions for all transistors.

Figure 6 shows the distribution of threshold voltages taken over all channels of all HP process chips at all common voltages. It is reasonably well fit to a Gaussian distribution, although there are tails caused by data taken at common voltages <2.5 V. When the data corresponding to common voltages below 2.5 V are removed (also shown in Figure 6), the distribution is well fit to a Gaussian with 11.6 mV RMS. Figure 7 shows the distribution of mean threshold voltage as a function of channel number, showing that there were no

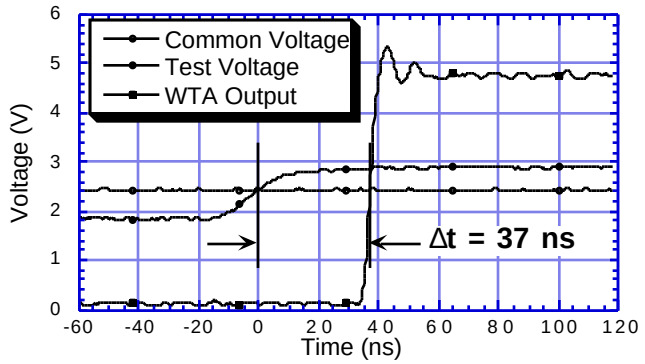

Figure 8: Propagation delay, measured from the time that a "test" input voltage crosses the common voltage until the WTA output bit changes state, for a single channel.

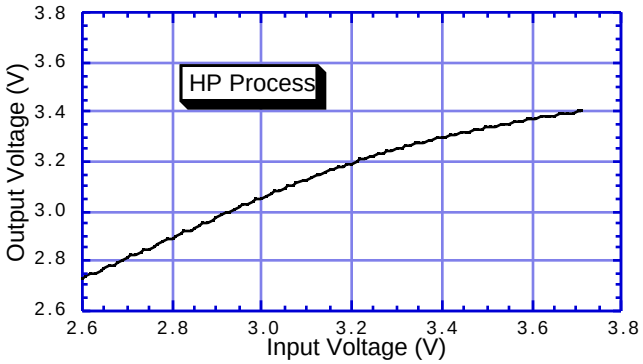

Figure 9: Mean analog output buffer output voltage as a function of input voltage, averaged over all channels of all HP chips. The channel to channel variation for each point is ≤8 mV RMS.

systematic threshold voltage differences between channels. The data in Figures 6&7 indicate that the performance of the individual channels are independent, suggesting that ICs can be fabricated with a larger number of channels, subject only to the 11.6 mV RMS channel to channel variations.

The propagation delay of the chip is measured by applying a common 2.5 V signal to 15 channels and a voltage ramp going from 1.8 V to 2.8 V in 30 ns to the 16th (test) channel. The WTA output bit corresponding to the test channel is monitored on an oscilloscope, and the time to change state after its input ramp voltage crosses the common voltage is measured, as shown in Figure 8. This propagation delay is virtually identical for the HP devices (37±1 ns for all channels of chips), but has significant channel to channel and chip to chip variations (48±15 ns) for the Orbit devices. While the propagation time is likely to depend on both the slew rate and the overdrive voltage of the test ramp, even the Orbit chips easily meet our <100 ns application requirement.

The performance of the analog output buffer is measured (for the HP chips only) by applying a common 2.5 V signal to 15 channels and a ≥2.6 V signal to the 16th (test) channel. The analog output of the winner (*i.e.* the test channel) is digitized and plotted as a function of the input voltage in Figure 9. While there is a 700 mV offset and some

nonlinearity above 3.2 V due to the voltage to current input converter, the nonlinearity is acceptable and the channel to channel variations are ≤8 mV RMS (all channels of all chips).

IV. Other Applications

Although this device was developed for a PET detector module, there are other applications that could benefit from the rapid identification of the maximum input voltage. Common themes for other potential applications are:

1) *Multi-Element Detector Arrays.* The WTA circuit is effectively a multiplexer, taking in the analog inputs of several elements and providing an analog output corresponding to the highest input, along with its digital address.

2) *Low Event Multiplicity.* The WTA is only capable of identifying a single channel at a time, so the detector array cannot have simultaneous signals in multiple channels that all need to be read out.

3) *Poor Signal to Noise Ratio.* An approach utilizing threshold discriminators would be simpler than the WTA provided that the signal was always above the threshold and the noise was always below the same threshold. However, when the signal to noise is poor, or when a single interaction causes spurious signal in other channels, the threshold discriminator approach is unreliable.

4) *High Event Rate.* An approach utilizing a microprocessor to search over multiple digitized inputs (perhaps with a scanning ADC to reduce electronics channel count) would be effective, but would have difficulty achieving event rates above 100 khz. The WTA approach can achieve rates above 10 Mhz.

A potential application is the readout of position sensitive photomultiplier tubes, which is presently done by determining a centroid in each of two views using a 16–18 resistor chain and current division [6]. This circuit could replace the resistor chain and current division circuit for determining the centroid [7]. This information could be used to restrict the channels used in the centroid calculation and result in a more accurate estimator, as only a few channels near the maximum channel contain useful signal and the remainder contain only noise. Anger cameras, such as those used for SPECT or in an alternate PET design [8], could conceivably employ a circuit such as this to identify the photomultiplier tube with the largest signal in order to accurately determine the position of the gamma ray interaction. This could reduce the number of ADCs used in a system (currently there tends to be one per photomultiplier tube) and hence its price. Another potential application is the readout of solid state detector arrays, such as double-sided CdZnTe micro-strip detectors used in coded-aperture telescopes for x-ray astronomy [9] .

V. Conclusions

We have manufactured a 16 channel prototype Winner Take All circuit that rapidly identifies (<50 ns) which input has the highest voltage, and provides both the digital address of this channel and an analog output voltage proportional to the highest input voltage. The main portion of the circuit (the Winner Take All) requires only two transistors per input channel and power consumption is low — ~0.5 mW independent of the number of input channels. Prototype circuits have been fabricated with two 1.2 µm CMOS processes and tested, and found to have reasonably good yield. The mean threshold voltage (*i.e.* the voltage difference required to reliably identify the input with the maximum voltage) was 19 mV with an 11.6 mV RMS deviation. The propagation delay is 37±1 ns for the HP devices and 48±15 ns for the Orbit devices. This circuit is useful for applications that wish to economically read out detector arrays that have low event multiplicity, high event rates, and poor signal to noise ratio.

VI. Acknowledgments

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VII. References

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